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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,810	02/27/2004	Leonard Forbes	1303.027US2	7846

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EXAMINER	
ANYA, IGWE U	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,810	FORBES, LEONARD	
	Examiner	Art Unit	
	Igwe U. Anya	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,8,12-15,17-19 and 26* is/are rejected.

7)☐ Claim(s) *5,6,9-11,16,20-25 and 27-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/27/04, 6/4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Beat (U.S Patent 5,959,465) ~~Noble et al. (US Patent 6124729)~~.

3. Beat teaches a method for forming a programmable logic array, comprising, forming a first logic plane that receives a number of input signals, wherein forming the first logic plane includes forming a number of logic cells arranged in rows and columns that are interconnected to provide a number of logical outputs, forming a second logic plane, wherein forming the second logic plane includes forming a number of logic cells arranged in rows and columns that receive the outputs of the first logic plane and that are interconnected to produce a number of logical outputs such that the programmable logic array implements a logical function, and forming the first logic plane and the second logic plane as NOR plane (fig. 7, & col. 9 lines 35 – 46);

wherein forming each of the logic cells includes, forming a first source/drain region and a second source/drain region separated by a channel region in a substrate,

forming a floating gate opposing the channel region and separated therefrom by a gate oxide, and forming a control gate opposing the floating gate. (fig. 8).

4. Claims 8, 12 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Noble et al. (US Patent 6124729).

5. Noble et al. teach a method for forming an in service programmable logic array, comprising, forming a plurality of input lines for receiving an input signal, forming a plurality of output lines, and forming one or more arrays having a first logic plane and a second logic plane connected between the input lines and the output lines, wherein forming the first logic plane and the second logic plane form a plurality of logic cells arranged in rows and columns for providing a sum-of-products term on the output lines responsive to the received input signal (figs. 1 – 3), wherein forming each logic cell includes forming a vertical non-volatile memory cell including:

forming a vertical pillar extending outwardly from a semiconductor substrate at intersections of the input lines and interconnect lines and at the intersections of the interconnect lines and the output lines (fig. 6A);

wherein each pillar includes a first source/drain region, a body region, and a second source/drain region (col. 9 lines 30 – 38);

forming a number of floating gates (fig. 4B, element 202) opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

forming a number of control gates (A_1) opposing the floating gates; and

forming a low tunnel barrier inter-gate insulator to separate the control gate from the floating gate; and

forming a number of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain regions of column adjacent pillars in the array (col. 9 lines 39 – 45).

forming each floating gate includes forming a vertical floating gate formed in a trench below a top surface of each pillar such that each trench houses a pair of floating gates opposing the body regions in adjacent pillars on opposing sides of the trench (fig. 5B elements 202).

forming the number of control gates includes forming the control gates in the trench below the top surface of the pillar and between the pair of floating gates, such that each trench houses a pair of control gates each addressing the floating gates one on opposing sides of the trench respectively, and wherein the pair of control gates are separated by an insulator layer (fig. 6B).

Claims 8, 12, 13, 15, 17, 18, 19 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Forbes (US Patent 6377070).

6. Forbes teaches a method for forming an in service programmable logic array, comprising, forming a plurality of input lines for receiving an input signal, forming a plurality of output lines, and forming one or more arrays having a first logic plane and a second logic plane connected between the input lines and the output lines, wherein forming the first logic plane and the second logic plane form a plurality of logic cells arranged in rows and columns for providing a sum-of-products term on the output lines

responsive to the received input signal, wherein forming each logic cell includes forming a vertical non-volatile memory cell including:

forming a vertical pillar extending outwardly from a semiconductor substrate at intersections of the input lines and interconnect lines and at the intersections of the interconnect lines and the output lines (fig. 5B);

wherein each pillar includes a first source/drain region, a body region, and a second source/drain region (fig. 5C);

forming a number of floating gates (642) opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

forming a number of control gates (662) opposing the floating gates; and

forming a low tunnel barrier inter-gate insulator (660) to separate the control gate from the floating gate; and

forming a number of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain regions of column adjacent pillars in the array (602).

forming each floating gate (763) includes forming a vertical floating gate formed in a trench below a top surface of each pillar such that each trench houses a pair of floating gates opposing the body regions in adjacent pillars on opposing sides of the trench (fig. 7F).

forming the number of control gates (862) includes forming the control gates in the trench below the top surface of the pillar and between the pair of floating gates, wherein each pair of floating gates shares a single control gate line, and wherein each

floating gate includes a vertically oriented floating gate having a vertical length of less than 100 nanometers (col. 10 lines 23 – 27);

forming the number of control gates (862) includes forming the control gates disposed vertically above the floating gates (fig. 8D element 863), and wherein each one of the pair of floating gates is addressed by an independent one of the number of control gates;

writing to one or more floating gates of a number of non-volatile memory cells in one or more arrays using channel hot electron injection; and

erasing charge from the one or more floating gates by tunneling electrons off of the one or more floating gates and onto the number of control gates.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2, 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beat (US Patent 5959465) in view of Bui (US Patent 6163049).

9. Beat teaches the features previously outlined, but lacks forming a low tunnel barrier inter-gate insulator of a metal oxide selected from the group consisting of lead oxide (Pb0) and aluminum oxide (Al_2O_3) to separate the control gate from the floating gate or a transition metal oxide insulator selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

10. However, Bui teaches forming a low tunnel barrier inter-gate insulator of a metal oxide selected from the group consisting of lead oxide (Pb0) and aluminum oxide (Al_2O_3) to separate the control gate from the floating gate or a transition metal oxide insulator selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5. (col. 4 lines 17 – 41).

11. Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate the teachings of Bui into the Beat reference to fabricate a NOR-NOR PLA with improved control and greater accuracy.

12. Claims 5, 6, 9, 10, 11, 16, 20 – 25, and 27 – 29 are objected to as being dependent upon a rejected claim, but would be allowable if rewritten in independent form.

13. Prior art considered, but not used in the rejection include Prall et al. (US Patent 6514842), Heybruck (US Patent 5488612), Lee et al. (USPAP 2002/0028541), Hseih (US Patent 4688078), and DiMaria et al. (US Patent 4939559).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Igwe U. Anya whose telephone number is (571) 272-1887. The examiner can normally be reached on M - F 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Igwe U. Anya
Examiner
Art Unit 2825

IA

August 7, 2004

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800